Specification Amendments

Please replace paragraph 005 with the following rewritten paragraph:

005 In particular, the undesirable effects of integrated circuit RC delay and signal crosstalk increase as integrated circuit densities increase, requiring increasingly low dielectric constants to decrease the parasitic capacitances of the dielectric insulating layers. For example, in design rule technologies of less than about 0.25 microns including 0.1 microns and lower, dielectric insulating layers having a dielectric constant of less than about 2.5, also referred to as ultra low-K dielectrics, are required to achieve acceptable circuit densities with reliable electrical behavior. Silicon dioxide based dielectric layers doped with carbon or organic substituents and forming an interconnecting porous structure within the SiO_2 matrix are increasingly desirable for forming IMD layers. Porous low-K materials have several drawbacks including enhanced absorption of chemical species ~~by~~ which may easily migrate throughout the IMD layer.

Please replace paragraph 007 with the following rewritten paragraph:

007 Another problem with low-K materials including carbon doping or carbon-silicon substituents in a silicon dioxide matrix ~~as~~ to form an IMD layer[[,]] relates to the common practice of subjecting the trench patterning photoresist to a plasma ashing process following the trench etching process. The plasma ashing process has been found to damage the low-K material by depleting the carbon from the IMD layer and thereby increasing the dielectric constant of the IMD layer. Various approaches to solving processing problems with low-K dielectrics have been proposed. One approach includes partially or substantially filling the via with a photoresist material prior to trench etching. This approach has met with difficulties due to the formation of etching resistant polymeric residues around the via opening following the trench etching process. Another approach has been to use hard masks or liners for etching the trench to avoid damage to the low-K IMD layer during the photoresist ashing process. This approach has the drawback of leading to enlarged (faceted) trench openings due to etching process chemistries that are not sufficiently selective to the low-K material. Increasing the hard mask layer thickness to prevent trench opening faceting in the trench etching process has been found to have the

undesirable effect of reducing surface planarity ~~including~~ as well as requiring increased~~ing~~ photoresist thickness over via portions in the trench pattering process thereby undesirably affecting patterning resolution.

Please replace the paragraph 0017 with the following rewritten paragraph:

0017 Still referring to Figure 1A, ~~formed~~ over the barrier layer 12 is formed a dielectric insulating layer 14, also referred to as an inter-metal dielectric (IMD) layer formed of, for example, ~~for example~~ a carbon doped silicon dioxide, also referred to as organo silicate glass (OSG) and C-oxide. Several commercially available formulations are available for producing the low-K carbon doped oxide, for example, known as SILK™ and BLACK DIAMOND™ according to conventional PECVD processes. In addition, the carbon doped oxides may be produced by PECVD methods using organo-silane precursors such as alkyl substituted cyclo-siloxanes where the dielectric constant may be varied over a range depending on the precursors and process conditions. The IMD layer is preferably formed having a dielectric constant less than about 2.5. Further, spin-on glass (SOG) low-K materials including silsesquioxanes, such as alkyl substituted silsesquioxanes, for example methyl-silsesquioxane (MSQ), may be

suitably used to form the IMD layer 14. Preferably, the IMD layer 14 is formed having a thickness of about 4000 to about 8000 Angstroms.

Please replace the paragraph 0020 with the following rewritten paragraph:

0020 Referring to Figure 1C, following anisotropically etching via openings e.g., 18, according to an aspect of the present invention, a first dielectric layer stack e.g., layer 20 including one or more layers of silicon oxide (e.g., SiO_2), silicon nitride (e.g., Si_3N_4), silicon oxynitride (e.g., SiON), silicon oxycarbide (e.g., SiOC), and hydrogenated silicon oxycarbide (SiOCH). The one or more dielectric layers, e.g., 18 are preferably deposited according to a first CVD process over the process surface including over the via openings, e.g., 18, to form at least one dielectric layer over the via opening level above the DARC layer 16 to close off and seal~~ing~~ an upper portion of the via opening 18. Preferably, the dielectric layer stack e.g., 20 is deposited to an overall thickness of about 1000 Angstroms to about 2000 Angstroms thickness above the DARC layer 16.